ABSTRACT OF THE DISCLOSURE

A device isolation structure and a method thereof including a semiconductor substrate wherein a field isolation region including a plurality of dummy active regions and an active region are defined, a plurality of trenches formed among the regions, a filling layer filled in the plurality of trenches, a gate insulation layer formed on the semiconductor substrate having the filling layer, and a second conduction layer formed on the gate insulation layer, is capable of preventing a dishing from being generated in etching by forming the plurality of dummy active regions in the field isolation region and basically preventing the wide trenches from being formed, minimizing a parasitic capacitance generated in the dummy active-gate insulation layer-gate insulation layer in the field isolation region, and simplifying an isolation process by using the dummy active pattern.